Translation

PCT/JP2003/016377

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference JFKR-78-PCT	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No. PCT/JP2003/016377	International filing date (*day/month/year*) 19 December 2003 (19.12.2003)	Priority date (*day/month/year*) 20 January 2003 (20.01.2003)
International Patent Classification (IPC) or national classification and IPC H05K 3/46, 1/02		
Applicant FUJIKURA LTD.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 9 sheets, including this cover sheet.

☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

These annexes consist of a total of _____ sheets.

3. This report contains indications relating to the following items:

- I ☒ Basis of the report
- II ☐ Priority
- III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- IV ☐ Lack of unity of invention
- V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI ☒ Certain documents cited
- VII ☐ Certain defects in the international application
- VIII ☐ Certain observations on the international application

Date of submission of the demand 08 July 2004 (08.07.2004)	Date of completion of this report 04 April 2005 (04.04.2005)
Name and mailing address of the IPEA/JP Facsimile No.	Authorized officer Telephone No.

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/JP2003/016377

I. Basis of the report

1. With regard to the **elements** of the international application:*

☒ the international application as originally filed

☐ the description:
pages _____, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

☐ the claims:
pages _____, as originally filed
pages _____, as amended (together with any statement under Article 19
pages _____, filed with the demand
pages _____, filed with the letter of _____

☐ the drawings:
pages _____, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

☐ the sequence listing part of the description:
pages _____, as originally filed
pages _____, filed with the demand
pages _____, filed with the letter of _____

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule 23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in written form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☐ The amendments have resulted in the cancellation of:

☐ the description, pages _____

☐ the claims, Nos. _____

☐ the drawings, sheets/fig _____

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

* *Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rule 70.16 and 70.17).*

** *Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/JP 03/16377

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	2, 4, 8-14, 17-45	YES
	Claims	1, 3, 5-7, 15, 16	NO
Inventive step (IS)	Claims	10, 11	YES
	Claims	1-9, 12-45	NO
Industrial applicability (IA)	Claims	1-45	YES
	Claims		NO

2. Citations and explanations

Document 1: JP 4-35092 A (Toshiba Corp.), 05 February 1992) & GB 2343995 A

Document 2: JP 2000-156564 A (NEC Corp.), 06 June 2000

Document 3: JP 4-94186 A (The Furukawa Electric Co., Ltd.), 26 March 1992

Document 4: JP 7-135375 A (Mitsui Toatsu Chemicals, Inc.), 23 May 1995

Document 5: JP 2000-183526 A (Matsushita Electric Industrial Co., Ltd.), 30 June 2000

Document 6: JP 8-139454 A (Toshiba Corp.), 31 May 1996

Document 7: JP 10-135595 A (Kyocera Corp.), 22 May 1998

Document 8: JP 2000-208667 A (Toshiba Corp.), 28 July 2000

Document 9: JP 2002-171063 A (Sony Chemicals Corp.), 14 June 2002

Document 10: JP 2002-43506 A (Kabushiki Kaisha North), 08 February 2002

Claims 1, 3, 5-7, 15 and 16

The inventions that are set forth in claims 1, 3, 5-7, 15 and 16 are disclosed in document 1 (page 2, lower right column, line 8 to page 3, upper right column, line 16 and fig. 1-2); therefore, the inventions in question lack novelty and do not involve an inventive step.

The inventions that are set forth in claims 2 and 17 do not involve an inventive step in the light of document 1 and document 2. It would be easy for a person skilled in the art to configure so that the substrate with a wiring circuit which is disclosed in document 1 is formed with dimensions that are smaller than the dimensions of the printed circuit motherboard, and is disposed upon the printed circuit motherboard in an insular manner, as disclosed in document 2 (paragraph [0016] and fig. 9-10).

The inventions that are set forth in claims 4, 13, 20, 22-24, 26, 27, 36-38, 43 and 44 do not involve an inventive step in the light of document 1 and document 3. It would be easy for a person skilled in the art to use the substrate with a wiring circuit on one surface wherein a conductive paste has been filled into the via holes, which is disclosed in document 3 (page 2, lower right column, line 9 to page 3, upper right column, line 11 and fig. 1-7), in the substrate with a wiring circuit from the multi-layered wiring board that is disclosed in document 1.

The inventions that are set forth in claims 8 and 19 do not involve an inventive step in the light of document 1 and document 4. It would be easy for a person skilled in the art to configure the multi-layered wiring board that is disclosed in document 1 so that a cover layer is formed thereupon, as disclosed in document 4 (paragraph [0014] and fig. 1).

The inventions that are set forth in claims 9 and 18 do not involve an inventive step in the light of document 1 and document 5. It would be easy for a person skilled in the art to configure the multi-layered wiring board that is disclosed in document 1 so that a cover layer is formed upon the portions other than the locations where the substrate with a wiring circuit has been disposed, as disclosed in document 5 (paragraph [0042] and fig. 3).

The invention that is set forth in claim 12 does not involve an inventive step in the light of document 1 and document 6. It would be easy for a person skilled in the art to configure the multi-layered wiring board that is disclosed in document 1 so that the insulating layer of the substrate with a wiring pattern functions as a cover layer for covering the printed circuit motherboard, as disclosed in document 6 (paragraphs [0014] and [0017], and fig. 1).

The invention that is set forth in claim 14 does not involve an inventive step in the light of document 1 and document 7. It would be easy for a person skilled in the art to configure the substrate with a wiring circuit which is disclosed in document 1 so that small holes are formed in the conductive layer and then a conductive paste is filled into the via holes, as disclosed in document 7 (paragraph [0009] and fig. 1).

The invention that is set forth in claim 21 does not involve an inventive step in the light of documents 1-3. It would be easy for a person skilled in the art to configure so that the substrate with a wiring circuit which is disclosed in document 1 is a substrate with a wiring circuit on one surface thereof, as disclosed in document 3, and is mounted in an insular manner, as disclosed in document 2.

The invention that is set forth in claim 25 does not involve an inventive step in the light of document 1, document 3 and document 4. It would be easy for a person skilled in the art to configure the multi-layered wiring board that is disclosed in document 1 so that the substrate with a wiring circuit is a substrate with a wiring circuit on one surface, as disclosed in document 3, and so that the printed circuit motherboard is covered by means of a cover layer, as disclosed in document 4.

The invention that is set forth in claim 28 does not

involve an inventive step in the light of document 1, document 3 and document 8. It would be easy for a person skilled in the art to configure so that the substrate with a wiring circuit which is disclosed in document 1 is a substrate with a wiring circuit on one surface, as disclosed in document 3, and is laminated to the printed circuit motherboard by means of a separation step or the like, as disclosed in document 8 (paragraphs [0017] to [0019]).

The inventions that are set forth in claims 29-31 and 33-35 do not involve an inventive step in the light of document 1 and document 9. It would be easy for a person skilled in the art to configure the primary surface of the circuit substrate that is disclosed in document 1 so that connection parts are formed by removing at least one portion of the insulating substrate, as disclosed in document 9 (paragraph [0023] to [0027] and fig. 1).

The invention that is set forth in claim 32 does not involve an inventive step in the light of document 1, document 2 and document 9. It would be easy for a person skilled in the art to configure so that the multi-layered wiring board that is disclosed in document 1 is disposed in an insular manner, as disclosed in document 2, and so that connection parts are formed by removing at least one portion of the insulating substrate from the substrate for the motherboard, as disclosed in document 9.

The invention that is set forth in claims 39 and 40 does not involve an inventive step in the light of document 1, document 3 and document 8. It would be easy for a person skilled in the art to configure the multi-layered wiring board that is disclosed in document 1 so that a substrate with a wiring circuit on one surface is used as the partially stratified substrate, as disclosed in document 3, and so that a conductive land part is provided in the outermost layer, as disclosed in document

8 (paragraph [0023] and fig. 6).

The invention that is set forth in claims 41 and 42 does not involve an inventive step in the light of document 1, document 3 and document 10. It would be easy for a person skilled in the art to configure the multi-layered wiring board that is disclosed in document 1 so that a substrate with a wiring circuit on one surface is used as the partially stratified substrate, as disclosed in document 3, and so that a contact hole is provided in the outermost layer, as disclosed in document 10 (paragraph [0050] and fig. 1).

The invention that is set forth in claim 45 does not involve an inventive step in the light of document 1 and document 8. It would be easy for a person skilled in the art to configure so that the substrate with a wiring circuit which is disclosed in document 1 is produced in the manner that is disclosed in document 8, wherein a plurality of substrates are formed, separated and laminated.

The invention that is set forth in claims 10 and 11 is not disclosed in any of the documents that are cited in the international search report; therefore, the invention in question is novel and involves an inventive step. A multi-layered wiring board that includes a cover layer comprising an opening at the location where the substrate with a wiring circuit is disposed, which is formed upon the printed circuit motherboard, wherein in order to prevent the conductive layer from being exposed to the outside, the wiring circuit on the printed circuit motherboard, which is exposed at the space between the cover layer and the substrate with a wiring circuit, is covered by means of a nobler metal, or the surface of the printed circuit motherboard, which is exposed at the space between the cover layer and the substrate with a wiring circuit, is covered by means of a second cover layer is

not disclosed in any of the documents that are cited in the international search report, and is not obvious to a person skilled in the art.

VI. Certain documents cited

1. Certain published documents (Rule 70.10)

Application No. Patent No.	Publication date *(day/month/year)*	Filing date *(day/month/year)*	Priority date (valid claim) *(day/month/year)*
JP 2003-229665 A	15 August 2003 (15.08.2003)	31 January 2002 (31.01.2002)	
[E,X]			

2. Non-written disclosures (Rule 70.9)

Kind of non-written disclosure	Date of non-written disclosure *(day/month/year)*	Date of written disclosure referring to non-written disclosure *(day/month/year)*